IN THE CLAIMS

1. (Currently Amended) An integrated circuit comprising:

a first switch, a second switch and a third switch;

a first conductor and a second conductor, each having different ~~first and second spans~~ first span and second span, respectively, along a first dimension, wherein the first span is greater than the second span, each of the first conductor and the second conductor being neither an input nor an output of a program controlled cell, at least one conductor of the first conductor and the second conductor to selectively couple to two independently controlled switches comprising the first switch and the second switch;

a first program controlled cell to drive the at least one conductor through the first switch without requiring traversal of another conductor;

a second program controlled cell to drive the at least one conductor through the second switch without requiring traversal of another conductor; and

wherein the first conductor is configured to drive the second conductor through [[a]] the third switch without requiring traversal of another conductor, and wherein the first conductor and the second conductor are spanning at least one common program controlled cell along the first dimension.

2. (Currently Amended) The integrated circuit as set forth in claim 1, wherein the first, second and third switches comprise program controlled passgates.

3. (Currently Amended) The integrated circuit as set forth in claim 1, wherein the first, second and third switches comprise program controlled drivers/receivers.

4. (Currently Amended) The integrated circuit as set forth in claim 1, wherein the first, second and third switches comprise program controlled passgates and program controlled drivers/receivers.

5. (Currently Amended) The integrated circuit as set forth in claim 1, wherein at least one of the first, second and third switches has a program controlled on state and off state.

6. (Previously Presented) The integrated circuit as set forth in claim 1, wherein the integrated circuit is implemented using process technology incorporating memory devices.

7. (Previously Presented) The integrated circuit as set forth in claim 1, wherein the integrated circuit is implemented using process technology incorporating non-volatile memory devices.

8. (Previously Presented) The integrated circuit as set forth in claim 1, wherein the integrated circuit is implemented using process technology incorporating fuse devices.

9. (Previously Presented) The integrated circuit as set forth in claim 1, wherein the integrated circuit is implemented using process technology incorporating anti-fuse devices.

10. (Previously Presented) The integrated circuit as set forth in claim 1, wherein the integrated circuit is implemented using process technology incorporating ferro-electric devices.

11. (Previously Presented) The integrated circuit as set forth in claim 1, further comprising a third conductor having a third span, the third conductor being neither an input nor an output of a program controlled cell.

12. (Previously Presented) The integrated circuit as set forth in claim 11, wherein the third conductor to selectively couple to the first conductor through a fourth switch without requiring traversal of another conductor.

13. (Previously Presented) The integrated circuit as set forth in claim 12, wherein the second span is equal to the third span and the third span is along the first dimension.

14. (Previously Presented) The integrated circuit as set forth in claim 13, wherein the second conductor spans at least one different program controlled cell than the third conductor along the first dimension.

15. (Previously Presented) The integrated circuit as set forth in claim 11, wherein the third span is along a second dimension.

16. (Previously Presented) The integrated circuit as set forth in claim 15, wherein the third conductor is configured to selectively couple to at least one conductor of the

first conductor and the second conductor through a fifth switch without requiring traversal of another conductor.

17. (Previously Presented) The integrated circuit as set forth in claim 16, wherein the third conductor is equal in span to the at least one conductor of the first conductor and the second conductor.

18. (Previously Presented) The integrated circuit as set forth in claim 11, wherein the first conductor, the second conductor and the third conductor have three different spans along the first dimension.

19. (Previously Presented) The integrated circuit as set forth in claim 18, wherein the second conductor is configured to selectively couple to the third conductor through a sixth switch without requiring traversal of another conductor.

20. (Previously Presented) The integrated circuit as set forth in claim 18, further comprising:

a fourth conductor having a fourth span along a second dimension;

a fifth conductor having a fifth span along the second dimension; and

a sixth conductor having a sixth span along the second dimension, the fourth, fifth and sixth spans being different than each other, and wherein each of the fourth, fifth and sixth conductors are neither an input nor an output of a program controlled cell.

21. (Previously Presented) The integrated circuit as set forth in claim 20, wherein at least one of the fourth, fifth and sixth conductors is configured to selectively

couple to at least one of the first, second and third conductors through a seventh switch without requiring traversal of another conductor.

22. (Previously Presented) The integrated circuit as set forth in claim 19, further comprising a fourth conductor having a fourth span, wherein the fourth conductor to selectively couple to at least one conductor of the first conductor, the second conductor and the third conductor through an eighth switch without requiring traversal of another span and the fourth conductor being neither an input nor an output of a program controlled cell.

23. (Previously Presented) The integrated circuit as set forth in claim 22, wherein the fourth span is along one of a dimension of a group consisting of the first dimension and the second dimension.

24. (Currently Amended) A method comprising:

providing a first conductor and a second conductor, each having different ~~first and second spans~~ first span and second span, respectively, along a first dimension, wherein the first span is greater ~~span~~ than the second span, each conductor of the first conductor and the second conductor being neither an input nor an output of a program controlled cell;

selectively coupling at least one conductor of the first conductor and the second conductor to two independently controlled switches comprising a first switch and a second switch;

driving the at least one conductor through the first switch without requiring traversal of another conductor, using a first program controlled cell;

driving the at least one conductor through the second switch without requiring traversal of another conductor using a second program controlled cell; and

selectively coupling the first conductor to drive the second conductor through a third switch without requiring traversal of another conductor, wherein the first conductor and the second conductor are spanning at least one common program controlled cell along the first dimension.

25. (Previously Presented) The method as set forth in claim 24, further comprising providing a third conductor having a third span, the third conductor being neither an input nor an output of a program controlled cell.

26. (Previously Presented) The method as set forth in claim 25, further comprising:

providing a fourth switch; and

selectively coupling the third conductor to the first conductor through the fourth switch without requiring traversal of another conductor.

27. (Previously Presented) The method as set forth in claim 26, wherein the second span is equal to the third span and wherein the third span is along the first dimension.

28. (Previously Presented) The method as set forth in claim 27, wherein the second conductor spans at least one different program controlled cell than the third conductor along the first dimension.

29. (Previously Presented) The method as set forth in claim 25, wherein the third span is along a second dimension.

30. (Previously Presented) The method as set forth in claim 29, further comprising:

providing a fifth switch; and

selectively coupling the third conductor to at least one conductor of the first conductor and the second conductor through the fifth switch without requiring traversal of another conductor.

31. (Previously Presented) The method as set forth in claim 30, wherein the third conductor is equal in span to the at least one conductor of the first conductor and the second conductor.

32. (Previously Presented) The method as set forth in claim 25, wherein the first span, the second span and the third span are three different spans along the first dimension.

33. (Previously Presented) The method as set forth in claim 32, further comprising:

providing a sixth switch; and

selectively coupling the second conductor to the third conductor through the sixth switch without requiring traversal of another conductor.

34. (Currently Amended) The method as set forth in claim 32, further comprising:

a fourth conductor having a fourth span along a second dimension;

a fifth conductor having a fifth span along the second dimension; and

a sixth conductor having a sixth span along the second dimension, the fourth, fifth and sixth spans being different than each other, and wherein each of the fourth, fifth and sixth conductors ~~are~~ being neither an input nor an output of a program controlled cell.

35. (Previously Presented) The method as set forth in claim 34, further comprising providing a seventh switch, at least one of the fourth, fifth and sixth conductors to selectively couple to at least one of the first, second and third conductors through the seventh switch without requiring traversal of another conductor.

36. (Previously Presented) The method as set forth in claim 33, further comprising providing a fourth conductor having a fourth span, wherein the fourth conductor to selectively couple to at least one conductor of the first conductor, the second conductor and the third conductor through an eighth switch without requiring traversal of another conductor and the fourth conductor being neither an input nor an output of a program controlled cell.

37. (Previously Presented) The method as set forth in claim 36, wherein the fourth span is along one of a dimension of a group consisting of the first dimension and the second dimension.

38. (Currently Amended) An integrated circuit comprising:

a first conductor and a second conductor, each having a different ~~first and second spans~~ first span and second span, respectively, along a first dimension, wherein the first conductor and the second conductor are spanning at least one common program controlled cell along the first dimension;

a third conductor having a third span along a second dimension, each of the first conductor, the second conductor and the third conductor being neither an input nor an output of a program controlled cell;

a first switch and a second switch, the first conductor to selectively couple to the third conductor through the first switch without requiring traversal of another conductor, and the second conductor to selectively couple to the first conductor through the second switch without requiring traversal of another conductor; ~~and~~

a third switch and a fourth switch, at least one conductor of the first conductor, the second conductor and the third conductor to selectively couple to two independently controlled switches comprising the third and the fourth switches;

a first program controlled cell to drive the at least one conductor through the third switch without requiring traversal of another conductor; and

a second program controlled cell to drive the at least one conductor through the fourth switch without requiring traversal of another conductor.

39. (Previously Presented) The integrated circuit as set forth in claim 38, wherein the first span is greater than the second span.

40. (Previously Presented) The integrated circuit as set forth in claim 38, wherein the second span is greater than the first span.

41. (Previously Presented) The integrated circuit as set forth in claim 40, further comprising a fourth conductor having a fourth span along the first dimension, wherein the fourth span is greater than the second span and the fourth conductor being neither an input nor an output of a program controlled cell.

42. (Currently Amended) The integrated circuit as set forth in claim 38, wherein the first, second, third and fourth switches comprise program controlled passgates.

43. (Currently Amended) The integrated circuit as set forth in claim 38, wherein the first, second, third and fourth switches comprise program controlled drivers/receivers.

44. (Currently Amended) The integrated circuit as set forth in claim 38, wherein the first, second, third and fourth switches comprise program controlled passgates and program controlled drivers/receivers.

45. (Currently Amended) The integrated circuit as set forth in claim 38, wherein at least one of the first, second, third and fourth switches has a program controlled on state and off state.

46. (Previously Presented) The integrated circuit as set forth in claim 38, wherein the integrated circuit is implemented using process technology incorporating memory devices.

47. (Previously Presented) The integrated circuit as set forth in claim 38, wherein the integrated circuit is implemented using process technology incorporating non-volatile memory devices.

48. (Previously Presented) The integrated circuit as set forth in claim 38, wherein the integrated circuit is implemented using process technology incorporating fuse devices.

49. (Previously Presented) The integrated circuit as set forth in claim 38, wherein the integrated circuit is implemented using process technology incorporating anti-fuse devices.

50. (Previously Presented) The integrated circuit as set forth in claim 38, wherein the integrated circuit is implemented using process technology incorporating ferro-electric devices.

51. (Previously Presented) The integrated circuit as set forth in claim 41, further comprising a fifth switch, the fourth conductor to selectively couple to the second conductor through the fifth switch without requiring traversal of another conductor.

52. (Currently Amended) A method comprising:

providing a first conductor and a second conductor, each having a different ~~first and second spans~~ first span and second span, respectively, along a first dimension, wherein each of the first conductor and the second conductor are spanning at least one common program controlled cell along the first dimension;

providing a third conductor having a third span along a second dimension, each conductor of the first conductor, the second conductor and the third conductor being neither an input nor an output of a program controlled cell;

selectively coupling the first conductor to the second conductor through a first switch without requiring traversal of another conductor;

selectively coupling the first conductor to the second conductor through a second switch without requiring traversal of another conductor; and

selectively coupling at least one conductor of the first conductor, the second conductor and the third conductor to ~~two~~ independently controlled ~~third and fourth switches~~ third switch and fourth switch;

driving the at least one conductor, using a first program controlled cell, through the third switch without requiring traversal of another conductor; and

driving the at least one conductor, using a second program controlled cell, through the fourth switch without requiring traversal of another conductor.

53. (Previously Presented) The method as set forth in claim 52, wherein the first span is greater than the second span.

54. (Previously Presented) The method as set forth in claim 52, wherein the second span is greater than the first span.

55. (Previously Presented) The method as set forth in claim 54, further comprising providing a fourth conductor having a fourth span along the first dimension, wherein the fourth span is greater than said second span and the fourth conductor is neither an input nor an output of a program controlled cell.

56. (Previously Presented) The method as set forth in claim 55, further comprising selectively coupling the fourth conductor to the second conductor through a fifth switch without requiring traversal of another conductor.

57. (Previously Presented) An integrated circuit comprising:

a first switch;

a first conductor, a second conductor and a third conductor, each having a respectively different first span, second span and third span along a first dimension, wherein the first span is greater than the second span, wherein the first span is greater than the third span, and wherein each of the first conductor, the second conductor and the third conductor spans at least one common program controlled cell along the first dimension;

a fourth conductor, a fifth conductor and a sixth conductor, each having a respectively different fourth span, fifth span and sixth span along a second dimension, wherein the fourth span is greater than the fifth span, wherein the fourth span is greater than the sixth span, and wherein each of the fourth conductor, the fifth conductor and the sixth conductor spans at least one common program controlled cell along the second dimension, the first conductor to selectively couple to the fourth conductor through the first switch without requiring traversal of another conductor; and

wherein each conductor of the first conductor, the second conductor, the third conductor, the fourth conductor, the fifth conductor and the sixth conductor is neither an input nor an output of a program controlled cell.

58. (Previously Presented) The integrated circuit as set forth in claim 57, further comprising a second switch, wherein the second conductor is configured to selectively couple to the fifth conductor through the second switch without requiring traversal of another conductor.

59. (Previously Presented) The integrated circuit as set forth in claim 57, wherein the first switch comprises program controlled passgates.

60. (Previously Presented) The integrated circuit as set forth in claim 57, wherein the first switch comprises program controlled drivers/receivers.

61. (Previously Presented) The integrated circuit as set forth in claim 57, wherein the first switch comprises program controlled passgates and program controlled drivers/receivers.

62. (Previously Presented) The integrated circuit as set forth in claim 57, wherein the first switch has a program controlled on state and off state.

63. (Previously Presented) The integrated circuit as set forth in claim 57, wherein the integrated circuit is implemented using process technology incorporating memory devices.

64. (Previously Presented) The integrated circuit as set forth in claim 57, wherein the integrated circuit is implemented using process technology incorporating non-volatile memory devices.

65. (Previously Presented) The integrated circuit as set forth in claim 57, wherein the integrated circuit is implemented using process technology incorporating fuse devices.

66. (Previously Presented) The integrated circuit as set forth in claim 57, wherein the integrated circuit is implemented using process technology incorporating anti-fuse devices.

67. (Currently Amended) A method comprising:

providing a first conductor, a second conductor and a third conductor, each having a respectively different first span, second span and third span along a first dimension, wherein the first span is greater than the second span, wherein the first span is greater than the third span, and wherein each of the first conductor, the second conductor and the third conductor ~~span~~ spans at least one common program controlled cell along the first dimension;

providing a fourth conductor, a fifth conductor and a sixth conductor having a respectively different fourth span, fifth span and sixth span along a second dimension, wherein the fourth span is greater than the fifth span, wherein the fourth span is greater than the sixth span, and wherein each of the fourth conductor, the fifth conductor and the sixth conductor ~~span~~ spans at least one common program controlled cell along the second dimension, each conductor of the first conductor, the second conductor, the third conductor, the fourth conductor, the fifth conductor and the sixth conductor being neither an input nor an output of a program controlled cell; and

selectively coupling the first conductor to the fourth conductor through a first switch without requiring traversal of another conductor.

68. (Previously Presented) The method as set forth in claim 67, further comprising selectively coupling the second conductor to the fifth conductor through a second switch without requiring traversal of another conductor.

69. (Currently Amended) An integrated circuit having a span, comprising:

a first switch;

a first conductor, a second conductor and a third conductor, each having a respectively different first span, second span and third span along a first dimension, wherein the first span is greater than at least one of the second span and the third span, wherein each of the first span, the second span and the third span is less than the span of the integrated circuit along the first dimension, and wherein the first conductor, the second conductor and the third conductor are spanning at least one common program controlled cell along the first dimension;

a fourth conductor and a fifth conductor having a respectively different fourth span and fifth span along a second dimension, wherein the fourth span is greater than the fifth span, wherein the fourth span is less than the span of the integrated circuit along the second dimension, and wherein the fourth conductor and the fifth conductor are spanning at least one common program controlled cell along the second dimension, the first conductor to selectively couple to the fourth conductor through the first switch without requiring traversal of another conductor; and

wherein each conductor of the first conductor, the second conductor, the third conductor, the fourth conductor and the fifth conductor is neither an input nor an output of a program controlled cell.

70. (Previously Presented) The integrated circuit as set forth in claim 69, further comprising a second switch, wherein the second conductor is configured to selectively couple to the fifth conductor through the second switch without requiring traversal of another conductor.

71. (Previously Presented) The integrated circuit as set forth in claim 69, wherein the integrated circuit consists of a core.

72. (Previously Presented) The integrated circuit as set forth in claim 69, wherein the integrated circuit consists of a core and I/O to core interfaces.

73. (Previously Presented) The integrated circuit as set forth in claim 69, wherein the integrated circuit excludes I/O logic blocks.

74. (Previously Presented) The integrated circuit as set forth in claim 69, wherein the integrated circuit excludes I/O logic blocks and I/O to core interfaces.

75. (Previously Presented) The integrated circuit as set forth in claim 69, wherein the first switch comprises program controlled passgates.

76. (Previously Presented) The integrated circuit as set forth in claim 69, wherein the first switch comprises program controlled drivers/receivers.

77. (Previously Presented) The integrated circuit as set forth in claim 69, wherein the first switch comprises program controlled passgates and program controlled drivers/receivers.

78. (Previously Presented) The integrated circuit as set forth in claim 69, wherein the first switch ~~comprises~~ has a program controlled on state and off state.

79. (Previously Presented) The integrated circuit as set forth in claim 69, wherein the integrated circuit is implemented using process technology incorporating memory devices.

80. (Previously Presented) The integrated circuit as set forth in claim 69, wherein the integrated circuit is implemented using process technology incorporating non-volatile memory devices.

81. (Previously Presented) The integrated circuit as set forth in claim 69, wherein the integrated circuit is implemented using process technology incorporating fuse devices.

82. (Previously Presented) The integrated circuit as set forth in claim 69, wherein the integrated circuit is implemented using process technology incorporating anti-fuse devices.

83. (Currently Amended) A method comprising:

providing a first conductor, a second conductor and a third conductor, each having a respective different first span, second span and third span along a first dimension, wherein the first span is greater than either the second span or the third span, and wherein each of the first conductor, the second conductor and the third conductor ~~are~~ is spanning at least one common program controlled cell along the first dimension;

providing a fourth conductor and a fifth conductor, each having a respectively different fourth span and fifth span along a second dimension, wherein the fourth span is greater than the fifth span, and wherein each of the fourth

conductor and the fifth conductor ~~are~~ is spanning at least one common program controlled cell along the second dimension;

each conductor of the first conductor, the second conductor, the third conductor, the fourth conductor and the fifth conductor being neither an input nor an output of a program controlled cell; and

selectively coupling the first conductor to the fourth conductor through a first switch without requiring traversal of another conductor.

84. (Previously Presented) The method as set forth in claim 83, further comprising selectively coupling the second conductor to the fifth conductor through a second switch without requiring traversal of another conductor.

85. (Previously Presented) The method as set forth in claim 83, wherein the integrated circuit consists of a core.

86. (Previously Presented) The method as set forth in claim 83, wherein the integrated circuit consists of a core and I/O to core interfaces.

87. (Previously Presented) The method as set forth in claim 83, wherein the integrated circuit excludes I/O logic blocks.

88. (Previously Presented) The method as set forth in claim 83, wherein the integrated circuit excludes I/O logic blocks and I/O to core interfaces.

89. (Previously Presented) The integrated circuit as set forth in claim 66, wherein the first switch consists of a single anti-fuse device.

90. (Previously Presented) The method as set forth in claim 67, wherein the first switch consists of a single anti-fuse device.

91. (Previously Presented) The integrated circuit as set forth in claim 74, wherein the first switch consists of a single anti-fuse device.

92. (Previously Presented) The method as set forth in claim 88, wherein the first switch consists of a single anti-fuse device.

93. (New) The integrated circuit as set forth in claim 58, wherein the first conductor, the second conductor, the third conductor, the fourth conductor, the fifth conductor, the sixth conductor, the first switch and the second switch are replicated, as a group, at least three times and wherein the at least three replicated groups are located along the first dimension or the second dimension.

94. (New) The integrated circuit as set forth in claim 58, wherein the first conductor, the second conductor, the third conductor, the fourth conductor, the fifth conductor, the sixth conductor, the first switch and the second switch are replicated, as a group, at least three times and wherein the at least three replicated groups are located, in a row, along the first dimension; and wherein the at least three replicated groups are replicated in the row at least three times and wherein the at least three replicated rows are located along the second dimension.

95. (New) The integrated circuit as set forth in claim 94, wherein a core of the integrated circuit comprises the at least three replicated rows.

96. (New) The integrated circuit as set forth in claim 95, wherein the core is exclusive of the conductors of I/O, I/O logic blocks, I/O to core, I/O to core interface, configuration control logic, clock lines and reset lines of the integrated circuit.

97. (New) The integrated circuit as set forth in claim 96, further comprising a third switch, a fourth switch and a fifth switch, wherein each conductor of the first conductor, the second conductor and the third conductor of a first replicated group of the at least three replicated groups of a first row of the at least three replicated rows to selectively couple to a respective conductor of equal span of an adjacent second replicated group of the at least three replicated groups of the first row along the first dimension through the respective third switch, fourth switch and fifth switch without requiring traversal of another conductor.

98. (New) The integrated circuit as set forth in claim 97, further comprising a sixth switch, a seventh switch and an eighth switch, wherein each conductor of the fourth conductor, the fifth conductor and the sixth conductor of the first replicated group of the at least three replicated groups of the first row to selectively couple to a respective conductor of equal span of an adjacent third replicated group of the at least three replicated groups of a second row of the at least three replicated rows along the second dimension through the respective sixth switch, seventh switch and eighth switch without requiring traversal of another conductor.

99. (New) The integrated circuit as set forth in claim 98, wherein at least one of the pluralities of the first switch and the second switch replicated along the first

dimension and the second dimension of the at least three replicated rows is implemented using process technology anti-fuse devices.

100. (New) The integrated circuit as set forth in claim 98, wherein at least one of the pluralities of the first switch and the second switch replicated along the first dimension and the second dimension of the at least three replicated rows is implemented using process technology incorporating memory devices.

101. (New) The integrated circuit as set forth in claim 98, wherein at least one of the pluralities of the first switch and the second switch replicated along the first dimension and the second dimension of the at least three replicated rows is implemented using process technology incorporating non-volatile memory devices.

102. (New) The method as set forth in claim 68, further comprising:

replicating, as a group, the first conductor, the second conductor, the third conductor, the fourth conductor, the fifth conductor, the sixth conductor, the first switch and the second switch a plurality of times along the first dimension or the second dimension.

103. (New) The method as set forth in claim 68, further comprising:

replicating, as a group, the first conductor, the second conductor, the third conductor, the fourth conductor, the fifth conductor, the sixth conductor, the first switch and the second switch at least three times and locating the at least three replicated groups, in a row, along the first dimension; and

replicating the at least three replicated groups in the row at least three times and locating the at least three replicated rows along the second dimension.

104. (New) The method as set forth in claim 103, wherein a core of the integrated circuit comprises the three replicated rows.

105. (New) The method as set forth in claim 104, wherein the core is exclusive of the conductors of I/O, I/O logic blocks, I/O to core, I/O to core interface, configuration control logic, clock lines and reset lines.

106. (New) The method as set forth in claim 105, further comprising:

providing a third switch, a fourth switch and a fifth switch; and

selectively coupling each conductor of the first conductor, the second conductor and the third conductor of a first replicated group of the at least three replicated groups of a first row to a respective conductor of equal span of an adjacent second replicated group of the at least three replicated groups of the first row along the first dimension through the respective third switch, fourth switch and fifth switch without requiring traversal of another conductor.

107. (New) The method as set forth in claim 106, further comprising:

providing a sixth switch, a seventh switch and an eighth switch; and

selectively coupling each conductor of the fourth conductor, the fifth conductor and the sixth conductor of the first replicated group of the at least three replicated groups of the first row to a respective conductor of equal span of an adjacent third replicated group of the at least three replicated groups of a second row along the

second dimension through the respective sixth switch, seventh switch and eighth switch without requiring traversal of another conductor.

108. (New) The method as set forth in claim 107, wherein at least one of the pluralities of the first switch and the second switch replicated along the first dimension and the second dimension of the at least three replicated rows is implemented using process technology incorporating anti-fuse devices.

109. (New) The method as set forth in claim 107, wherein at least one of the pluralities of the first switch and the second switch replicated along the first dimension and the second dimension of the at least three replicated rows is implemented using process technology incorporating memory devices.

110. (New) The method as set forth in claim 107, wherein at least one of the pluralities of the first switch and the second switch replicated along the first dimension and the second dimension of the at least three replicated rows is implemented using process technology incorporating non-volatile memory devices.